WHAT IS CLAIMED IS:

1. A magnetic memory comprising:

first and second memory cells;

a read controller coupled to the first and second memory cells, wherein the read controller is configured to provide a read clock signal to initiate the next read operation at a preselected period, wherein the read clock signal period is a multiple of a system clock signal period; and

an output controller coupled to the read controller and to the first and second memory cells, wherein the output controller is configured to receive read data in parallel only from the first or second memory cells which have completed the current read operation regardless of whether both the first and second memory cells have completed the current read operation and convert the parallel data to serial data and shift the parallel data to an output in synchronism with the system clock signal.

2. The memory of claim 1, wherein the read controller has a first and second preselected state, wherein when the read controller is in the first state, the next read operation is initiated in synchronism with the read clock signal for both the first and second memory cells when the current read operation is complete for both the first and second memory cells, and when the read controller is in the second state, the next read operation is initiated in synchronism with the read clock signal for only the first or second memory cells which have completed the current read operation.

3. The memory of claim 2, wherein the read controller includes:

counter logic configured to provide the read clock signal at the preselected period; and

read logic coupled to the counter logic, wherein the read logic is configured to initiate the next read operation for the first or second memory cells

which have completed the current read operation, wherein the next read operation is initiated in synchronism with the read clock signal.

4. The memory of claim 3, wherein the counter logic includes:

a register configured to store a delay value corresponding to the preselected read clock signal period; and

a programmable counter coupled to the register and to the system clock, wherein the programmable counter is configured to provide the read clock signal at the period which is a multiple of a system clock signal period.

5. The memory of claim 4, wherein the programmable counter counts system clock signal cycles and compares a count of the system clock signal cycles to the delay value after each cycle, wherein the counter provides the read clock signal when the count of the system clock signal cycles is equal to the delay value, and wherein the counter is reset by the read clock signal.

6. The memory of claim 3, wherein the read logic includes

a first logic device including a first input coupled to the counter logic, wherein the first logic device is configured to initiate the next read operation in synchronism with the read clock signal for the first memory cell if the current read operation is complete for the first memory cell; and

a second logic device including a first input coupled to the counter logic, wherein the second logic device is configured to initiate the next read operation in synchronism with the read clock signal for the second memory cell if the current read operation is complete for the second memory cell.

7. The memory of claim 6, wherein the read logic includes:

a third logic device including a first input coupled to the counter logic, wherein the third logic device is configured to initiate the next read operation in synchronism with the read clock signal for both the first and second memory

cells when the current read operation is complete for both the first and second memory cells.

8. The memory of claim 7, wherein the read logic includes:

a fourth logic device including an input coupled to an output of the first logic device;

a fifth logic device including an input coupled to an output of the second logic device; and

an inverter, wherein an input of the inverter and a third input of the first and second logic devices are coupled to a read mode select input which preselects the first or second state, wherein an output of the inverter is coupled to a fourth input of the third logic device, wherein when the read mode input selects the first state, the fourth and fifth logic devices are configured to initiate the next read operation in synchronism with the read clock signal for both the first and second memory cells when the current read operation is complete for both the first and second memory cells, and wherein when the read mode input selects the second state, the fourth and fifth logic devices are configured to initiate the next read operation in synchronism with the read clock signal for the first or second memory cells which have completed the current read operation.

9. The memory of claim 8, wherein the first, second, third, fourth and fifth logic devices are NAND gates.

10. The memory of claim 2, wherein the output controller includes:

a first register coupled to the first memory cell and the counter logic, wherein the first register is configured to store a first read data from the first memory cell which has completed the current read operation in synchronism with the read clock signal;

a second register coupled to the second memory cell and the counter logic, wherein the second register is configured to store a second read data from

the second memory cell which has completed the current read operation in synchronism with the read clock signal; and

parallel-to-serial shift logic coupled to the first and second registers, wherein the parallel-to-serial shift logic is configured to store the first or second read data in synchronism with the read clock signal for the first or second memory cell which have completed a prior read operation, and wherein the parallel-to-serial shift logic is configured to shift to an output the stored first or second read data in synchronism with the system clock signal.

11. The memory of claim 10, wherein the first register includes a first tag, wherein the first tag provides an address location for the first read data, and wherein the parallel-to-serial shift logic shifts the first tag and the corresponding stored first data together to the output in synchronism with the system clock signal.

12. The memory of claim 11, wherein the second register includes a second tag, wherein the second tag provides an address location for the second read data, and wherein the parallel-to-serial shift logic shifts the second tag and the corresponding stored second data together to the output in synchronism with the system clock signal.

13. A magnetic memory storage device, comprising:

an array of memory cells;

an array of bit lines extending in a first direction which intersects the array of memory cells;

an array of word lines extending in a second direction which intersects the array of memory cells;

at least two column drivers coupled to the bit lines;

at least two sense amplifiers coupled to the column drivers; and

a control circuit coupled to the column drivers and the sense amplifiers, wherein the control circuit is configured to individually control read operations

for each column driver, including a read control circuit coupled to the column drivers, wherein the read control circuit is configured to initiate a next read operation for each of the column drivers which have completed a current read operation, and an output control circuit coupled to the read control circuit and the sense amplifiers, wherein the output control circuit is configured to receive read data in parallel from the sense amplifiers corresponding to the column drivers which have completed the current read operation and convert the parallel data to serial data in synchronism with the read clock signal.

14. The magnetic memory storage device of claim 13, wherein the read control circuit has a first and second preselected state, wherein when the read control circuit is in the first state, the next read operation is initiated in synchronism with a read clock for all of the column drivers when all of the column drivers have completed the current read operation, and wherein when the read control circuit is in the second state, the read operation is indicated in synchronism with the read clock signal for the column drivers which have completed the current read operation.

15. The magnetic memory storage device of claim 14, wherein the read control circuit includes:

a counter circuit configured to provide the read clock signal, wherein the read clock signal has a preselected period; and

a read circuit coupled to the counter circuit, wherein the read circuit is configured to initiate the next read operation for the column drivers which have completed the current read operation, wherein the next read operation is initiated in synchronism with the read clock signal, wherein the output control circuit includes:

at least two register circuits coupled to the sense amplifiers and the counter circuit, wherein each register circuit is configured to store read data in synchronism with the read clock signal for corresponding column drivers which have completed a current read operation; and

a parallel-to-serial shift circuit coupled to the register circuits, wherein the parallel-to-serial shift circuit is configured to store the read data in synchronism with the read clock signal for the column blocks which have completed a prior read operation, wherein the parallel-to-serial shift circuit is configured to shift to an output the stored read data in synchronism with the system clock signal, wherein each of the registers includes a tag, wherein the tag provides an address location for corresponding stored read data, and wherein the parallel-to-serial shift circuit shifts the tag and the corresponding stored read data together to the output in synchronism with the system clock signal.

16. The magnetic memory storage device of claim 25, wherein each sense amplifier includes a read status circuit which is configured to enable the corresponding register circuit to store the read data in synchronism with the read clock signal when the current read operation is complete, and wherein the read status circuit of at least one of the at least two sense amplifiers is configured to enable one or more other ones of the at least two sense amplifiers to initiate the next read operation in synchronism with the read clock signal after the next read operation has been initiated for the at least one of the at least two sense amplifiers.

17. A magnetic memory comprising:

first and second memory cells; and

means coupled to the first and second memory cells, wherein the means individually controls read operations for each of the first and second memory cells, including wherein the control means comprises:

a read means coupled to the first and second memory cells, wherein the read means is configured to initiate a next read operation only for the first or second memory cells which have completed a current read operation, output means coupled to the read means and the first and second memory cells, wherein the output means is configured to receive read data in parallel from the first or second memory cells which have completed the current read operation and

convert the parallel data to serial data in synchronism with the next read operation.

18. The magnetic memory of claim 17, wherein the read means includes a system clock, wherein the read means is configured to provide a read clock signal to initiate the next read operation at a preselected period, wherein a read clock signal period is a multiple of a system clock signal period.

19. The magnetic memory of claim 18, wherein the read means has a first and second preselected state, wherein when the read means is in the first state, the next read operation is initiated in synchronism with the read clock signal for both the first and second memory cells when the current read operation is complete for both the first and second memory cells, and wherein when the read means is in the second state, the next read operation is initiated in synchronism with the read clock signal for the first or second memory cells which have completed the current read operation.

20. A method of controlling a read operation in a magnetic memory, the method comprising:

initiating a current read operation only for first and second memory cell;

receiving read data in parallel from the first or second memory cells which have completed the current read operation;

converting the parallel read data to serial data in synchronism with the initiation of the next read operation; and

initiating a next read operation for the first or second memory cells which have completed a current read operation, regardless of whether both the first or second memory cells have completed the current read operation.

21. The method of claim 20, further comprising:

providing a system clock; and

providing a read clock signal to initiate the next read operation at a preselected period, wherein a read clock signal period is a multiple of a system clock signal period.

22. The method of claim 21, further comprising:

initiating the next read operation in synchronism with the read clock signal for both the first and second memory cells when the current read operation is complete for both the first and second memory cells

23. The method of claim 41, further comprising:

initiating the next read operation in synchronism with the read clock signal for the first or second memory cells which have completed the current read operation.